Monolithic Voltage Controlled Oscillator for *X*- and *Ku*-Bands

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Abstract —A GaAs voltage controlled oscillator circuit that tunes from 11.15 to 14.39 GHz and 16 to 18.74 GHz has been designed and fabricated. The 1.1 mm × 1.2-mm chip includes two varactors, a 300-μm FET, bypass capacitors, tuning inductors, and isolation resistors. Wide-band circuit design techniques will be described. Varactor and circuit effects causing the noncontinuous bandwidth will be discussed showing the capability of continuous 11 to 18 GHz tuning using a single GaAs chip.

I. Introduction

MAJOR EMPHASIS in the past 5 years in monolithic GaAs circuits has been in amplifier, mixer, T/R switch, and phase shifter networks while oscillator development has continued to be hybrid oriented. The first microwave monolithic oscillator above *L*-band including both the power generating and tuning elements on a single chip was previously reported by the authors [1]. This circuit covered 8.8 to 10 GHz. The present work allows two varactors to be implemented, one in the source and one in the gate circuits has given a tuning bandwidth covering 11.15 to 14.39 GHz and 16 to 18.74 GHz from a single chip. This circuit demonstrates the capability to cover *X*- and *Ku*-bands continuously with one monolithic circuit. The design technique used and a description of the unique varactor are summarized with an explanation relating to the varactor *Q* which created the frequency gap between 14.39 and 16 GHz.

II. Circuit Design

The negative impedances required to cause oscillations in a MESFET are a result of positive feedback. If the correct feedback reactance is added to a properly selected device configuration, oscillations can occur from very low frequencies to approximately f_{max} of the active device. After comparing the possible combinations both analytically and experimentally, the common gate configuration utilizing an inductive reactance between gate and ground as the regenerative feedback element was selected due to its inherent broad-band negative resistances and ease of analysis. A varactor was placed in series with the inductor to tune the negative impedances across a wide bandwidth.

In order to make design tradeoffs between the tuning circuit topologies and arrive at element values which would produce a wide bandwidth oscillator, several simplifying assumptions were required. Since oscillations build up from small signal conditions, small signal *S*-parameters were used to characterize the FET, and this data was then used to predict tuning bandwidths. Experimental verification showed reasonable correlation to the *S*-parameter analysis. Nonlinear device behavior due to large signal operation of the device was assumed to be primarily a change in source–drain resistance which does not appreciably change the phase angle or magnitude of the negative impedances appearing at the source with the drain appropriately loaded as in the case of this common gate design. Use of a large signal model confirmed this assumption while showing that there is a shift downward in frequency due to large signal

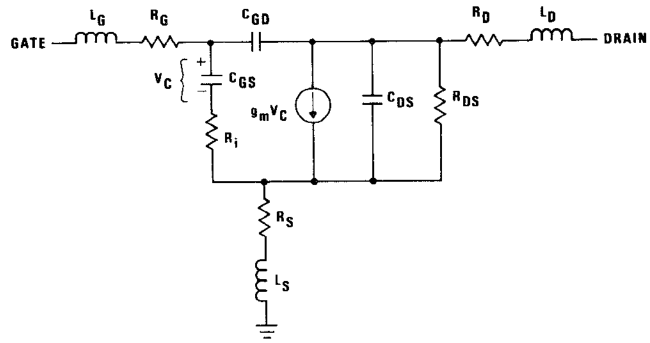

Fig. 1. FET model schematic.

TABLE I
FET Model Element Values

Element	Value
L_G	0.15 nH
R_G	7.43 Ω
C_{GS}	0.338 pF
R_i	0.100 Ω
C_{GD}	0.028 pF
C_{DS}	0.097 pF
R_{DS}	215 Ω
R_D	1.04 Ω
L_D	0.244 nH
R_S	4.9 Ω
L_S	0.077 nH
gm	37 m℧
τ	2.65 ps

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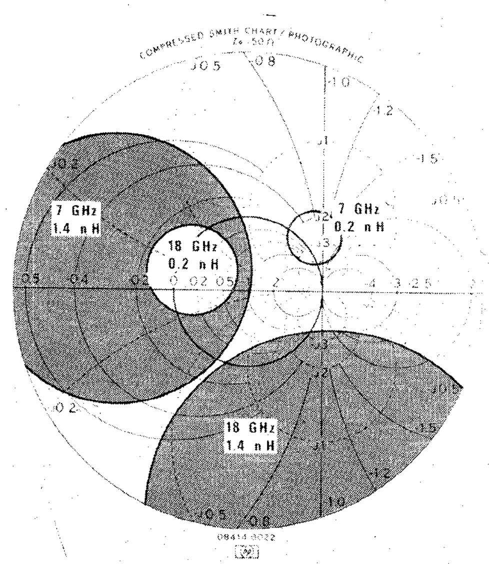

Fig. 2. Stability circles for 0.2-nH and 1.4-nH gate inductance.

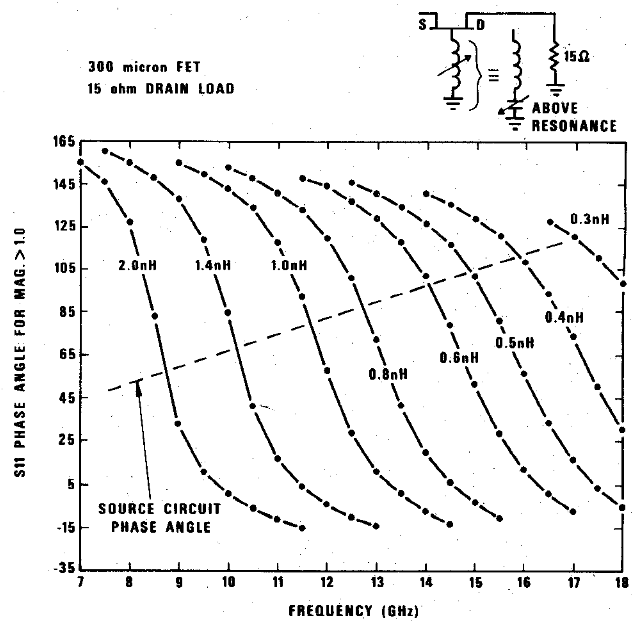

Fig. 3. FET source reflection coefficient.

operation; however, this downward shift in frequency does not appreciably affect bandwidth analysis. A design technique that allowed representative bandwidth and element value predictions was developed that entails characterization of the device by S-parameter measurements, stability circle analysis, drain circuit definition, computer generation of composite S-parameters utilizing the selected drain circuit, and source circuit phase angle graphs which allow bandwidth and element value selection.

To perform this bandwidth analysis, first S-parameters are taken on a common source MESFET and a model is fit to the data. Fig. 1 shows the common source FET model used, and Table I gives the associated element values for a 300-μm device after a fit has been performed on measured S-parameter data. Using computer aided design, the model is transformed to a common gate device with a series gate feedback inductor and stability circles are generated for varying values of this gate inductance as shown in Fig. 2. This family of circles defines the region of impedances that the drain must see to maintain negative source resistances as the gate-feedback inductance is varied. A 15-Ω drain load will allow negative resistances to appear at 11 GHz with 1.2-nH net inductance in the gate and will also allow negative source resistances at 18 GHz if that net gate inductance is changed to 0.2 nH.

Maintaining negative impedances at the source makes it possible to terminate that port using an appropriate passive phase cancellation network that will allow oscillation to occur. Tuning is accomplished by varying the impedance (net inductive reactance) from gate to ground. The frequency at which negative impedance is seen at the source for a given gate inductance and drain matching network is the frequency at which free-running oscillations will occur (assuming an appropriate phase cancellation network is used to terminate the source). The relative magnitude of that negative impedance is an indication of the amount of tuning element (varactor) loss that can be tolerated and the amount of output power that can be obtained. Table II gives the source reflection coefficients of the common gate FET model as described earlier with the

TABLE II
SOURCE REFLECTION COEFFICIENT FOR SPECIFIED GATE INDUCTANCES

Frequency	FET Source Reflection Coefficient for Specified Gate Inductances		
	.2 nH	.6 nH	1.0 nH
8.0 GHz			$0.7\angle 163$
9.0			$1.0\angle 155$
10.0			$1.6\angle 143$
11.0		$0.9\angle 153$	$2.8\angle 119$
12.0		$1.2\angle 144$	$3.9\angle 58$
13.0		$1.7\angle 130$	$2.3\angle 12$
14.0		$2.5\angle 102$	$1.4\angle -7$
15.0		$2.8\angle 52$	$1.1\angle -13$
16.0	$0.9\angle 134$	$1.8\angle 13$	$0.9\angle -17$
17.0	$1.2\angle 121$	$1.1\angle -7$	
18.0	$1.5\angle 99$	$0.7\angle -19$	

gate feedback inductance values of 0.2 nH, 0.6 nH, and 1.0 nH. The drain was loaded into 15-Ω real. The change in gate inductance clearly gives a change in the frequency at which negative impedances occur and in the phase angle.

The family of curves generated using the above analysis is given in Fig. 3. The abscissa is the phase angle of the source reflection coefficient (when it is greater than unity) with the drain loaded into a 15- to 50-Ω two-section transformer. From these data it was determined that a capacitive termination is required in the source network to cancel the imaginary part of the FET source impedance. The circuit then oscillates at that frequency where the source phase angle is cancelled and negative impedance is seen at the source. The bandwidth may be determined by calculation of the terminating network's phase angle slope;

the intersection of this slope and the varying gate inductance family (given by the net gate inductance value as the series varactor capacitance changes) gives the tuning bandwidth.

Several hybrid oscillator circuits were built using this analytical approach. Results showed that selection of varactor values to achieve a particular bandwidth was possible. The frequency of oscillation was also predictable from use of this method for other circuit element value selection.

Oscillator circuits utilizing one varactor in the gate and optimally terminated at the other two ports will give maximum tuning bandwidths of 4 GHz at X-band [2], [3]. The tuning curves were used to study improvements in the source network which would increase tuning bandwidth. A varactor was added to the source network so that the phase angle could be tuned radically versus frequency, thus improving the obtainable VCO bandwidth by more than 2.5 GHz.

Fig. 4 shows phase versus frequency data for the source network shown in the figure. As the varactor is tuned, the phase changes rapidly. If Fig. 5 is considered to exemplify the FET phase angle requirements for oscillation then at 10.5 GHz with 1.0 nH in the gate, a phase angle of approximately $-130°$ is required at the source circuit. As the source varactor (gate varactor value held constant) is tuned, the source would follow the dotted line on Fig. 4 since the oscillator would ride the 1.0-nH line given in Fig. 5. At a source varactor value equal to 0.3 pF the frequency of the oscillation would be 12.5 GHz. If the gate varactor is now tuned (source varactor held constant while the gate varactor is tuned) the frequency of oscillation will follow the source phase curve given by the 0.3-pF line in Fig. 4. This source and gate tuning path is given by the dotted line in Fig. 5 which shows the source tuning the oscillator from 10.5 GHz to 12.5 GHz (with a source varactor swing of 0.7 pF and 0.28 pF) and the gate varactor tuning the oscillator from 12.5 GHz to 18 GHz (with a gate varactor swing of 1.0 pF to 0.10 pF). Table III gives the values of gate inductance and source circuit varactor capacitance for selected frequencies. This example simply illustrates the basic tuning mechanisms and does not include all circuit parameter considerations required for proper analysis.

This varactor analysis which was developed at Texas Instruments has allowed TI to establish state-of-the-art tuning bandwidths for hybrid varactor tuned VCO's [4]. This technique allows a practical estimation of varactor swing and the circuit element values required for a given bandwidth.

Recently, efforts have been made to incorporate the FET, varactors, and capacitor on one piece of GaAs, thus reducing the present 6-mm × 6-mm hybrid oscillator circuit at X-band to 1.1 mm × 1.2 mm. This reduced the number of bond wires and assembly steps required by a factor of five to ten times.

A circuit to obtain oscillations in X- and Ku-band was generated for monolithic implementation with the schematic given in Fig. 6. the 15- to 50-Ω transformer was not placed on the mask for the GaAs chip in order to maximize the number of oscillator circuits obtained from each slice. Isolation resistors were included on the chip to reduce the

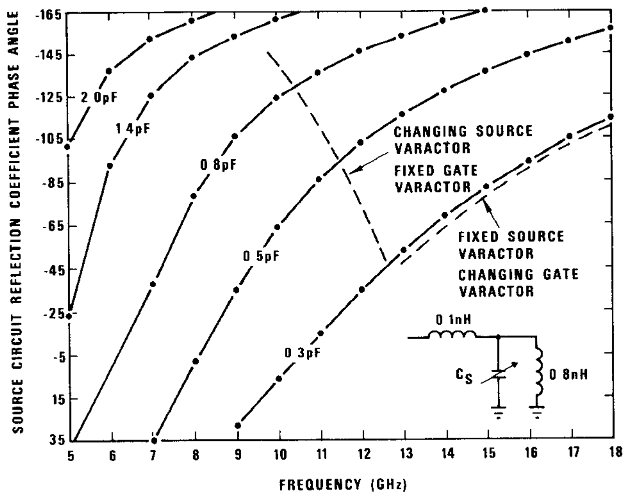

Fig. 4. Source circuit reflection coefficient phase versus frequency.

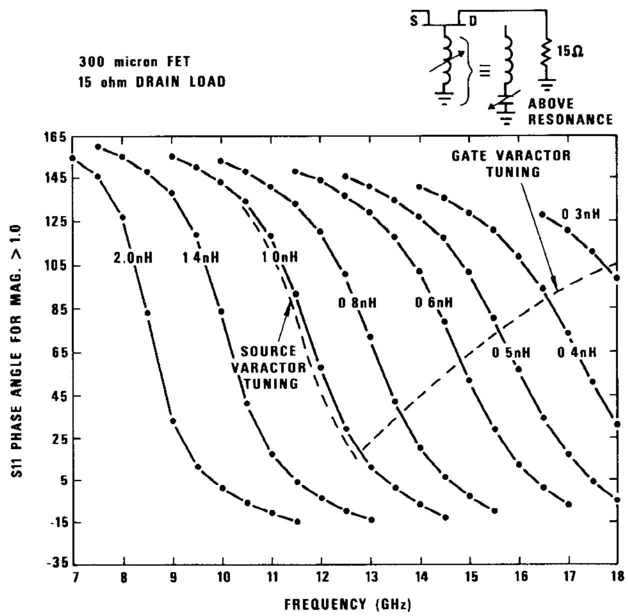

Fig. 5. Two varactor oscillator source reflection coefficient.

TABLE III
GATE INDUCTANCES AND SOURCE CIRCUIT VARACTOR CAPACITANCES FOR SELECTED FREQUENCIES

Frequency (GHz)	L_G* (nH)	C_s (pF)
10.5	1.0	0.9
12.0	1.0	0.4
12.5	1.0	0.3
13.0	0.9	0.28
15.0	0.58	0.28
17.0	0.36	0.28
18.0	0.29	0.28

* L_G is actually a series L-C network where the capacitor is a varactor and the inductor is fixed.

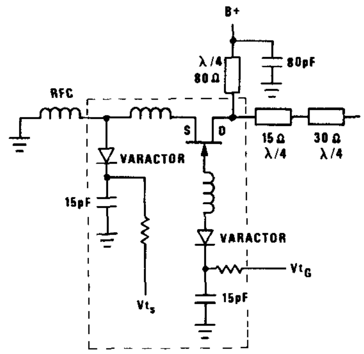

Fig. 6. VCO schematic.

chance of low frequency oscillations and to serve as current limiting resistors if the varactor diodes should be accidently forward biased.

III. Monolithic Varactor Diode

Conventional varactor diodes, particularly those with large tuning ratios (hyperabrupt diodes) require highly conductive substrate material and relatively thick epitaxial layers (>1 μm). These materials requirements are not compatible with those for GaAs FET-based monolithic microwave integrated circuits (MMIC's) which require a thin (<0.05 μm), uniformly doped active layer on a semi-insulating substrate. To integrate the conventional hyperabrupt diode on a semi-insulating substrate requires a very complicated selective epitaxial deposition. The materials required to fabricate the diode discussed here are the same as or very similar to those for the FET, so this device type will be extremely important in monolithic voltage controlled oscillators.

Van Tuyl [5] has reported the use of a GaAs varactor diode in an MMIC which is similar in design and materials requirements to that discussed here. This device does not however, provide the same wide-band capacitance tuning characteristics. This wide tuning range ($C/C_0>10$) is essential for many microwave applications.

The device discussed here is an interdigitated Schottky-barrier diode and was reported on by the authors previously [6]. The key feature of the diode is that an arbitrarily high capacitance ratio is achieved by the change in the effective junction area as the depletion layer punches through on the semi-insulating substrate. A simple, uniformly doped n-layer on a Cr-doped or other semi-insulating GaAs substrate can be used. The layer thickness and/or the amount of anode recess is chosen to allow punch-through before breakdown. The diode consists of one or more Schottky-barrier anode fingers spaced betweeen ohmic cathode regions. An n-type GaAs layer is defined by mesa etching and other means so that it is only under the active area. The bond pads (or interconnects to other parts of a monolithic circuit) are located on the semi-insulating substrate for minimum parasitic capacitance and conductance.

The key feature of the device is illustrated in Fig. 7. The doping-thickness product of the n-layer under the anode is selected so that punch-through to the substrate occurs prior to breakdown. A rapid drop in capacitance occurs at

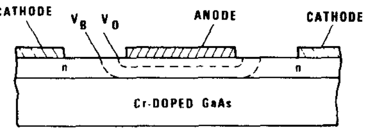

Fig. 7. Monolithic varactor.

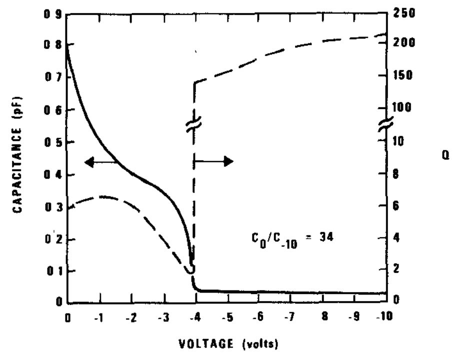

Fig. 8. Theoretical $C-V$ and Q for a monolithic varactor.

punch-through because the effective area of the diode is reduced to that of the depletion layer sidewalls alone. The fractional drop in capacitance is related to the ratio of the anode length (direction parallel to current flow) and the layer thickness. The series resistance is related to the anode length and anode-cathode spacing.

The region beneath the anode prior to punch-through can be regarded as a distributed RC network. On that basis the equivalent terminal impedance can be calculated. The equivalent resistance R_e and capacitance C_e are given by

$$R_e=1/2\sqrt{\frac{R_0}{2\omega C_0}}\left(\frac{(\sinh\theta-\sin\theta)}{(\cosh\theta-\cos\theta)}\right)+1/2R_s \quad (1)$$

$$\frac{1}{\omega C_e}=1/2\sqrt{\frac{R_0}{2\omega C_0}}\left(\frac{(\sinh\theta+\sin\theta)}{(\cosh\theta-\cos\theta)}\right) \quad (2)$$

where $\theta=L\sqrt{1/2\omega R_0C_0}$, R_s is the parasitic series resistance to the cathode on each side, and R_0 and C_0 are the resistance and capacitance per unit length under the anode. These equations do not include the sidewall capacitance, which were added in separately for biases near punch-through.

Using (1) and (2), the $C-V$ characteristic, the series resistance and $Q(=1/\omega R_eC_e)$ at 10 GHz have been calculated for several appropriate diode designs. Fig. 8 shows the $C-V$ characteristics and Q for a 6-μm$\times$100-μm anode device. In this case the Q is 6 at zero bias and drops below 2 before punch through at approximately 3.8 V. It is this sharp reduction in Q and a high surface leakage path on this slice of monolithic oscillators that caused the drop in power output in the center of the frequency band.

IV. Experimental Results

A. Tuning Bandwidth

The varactor diodes, a 300-μm FET, and the associated circuitry discussed earlier were implemented on a single GaAs 1.1-mm$\times$1.2-mm chip as shown in Fig. 9. The

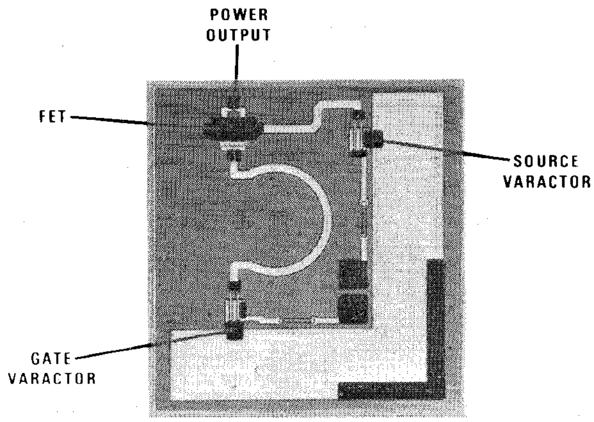

Fig. 9. Monolithic VCO photograph.

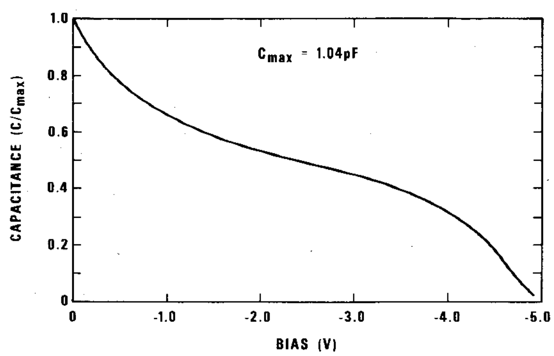

Fig. 10. Experimental $C-V$ characteristics for a monolithic varactor.

varactor diodes were designed for a 1.0-pF starting value and a capacitance ratio greater than 15 : 1. Fig. 10 gives the $C-V$ characteristics for the actual diode. Figs. 11 and 12 show the frequency and power respectively versus tuning voltage of an oscillator as first the varactor in the source was tuned from 0 to 9 V, and then the varactor in the gate was tuned 0 to 17 V. The actual voltage across the varactor was less in each case due to the voltage drop across the 2-kΩ resistor as the varactor became leaky. The oscillator tuned smoothly from 11.15 to 14.39 GHz where the oscillations ceased due to the low Q and excessive surface leakage across the diode. As the tuning voltage was increased on the gate to 3.2 V the oscillation began once again at 16.0 GHz and continued tuning to 18.74 GHz.

B. Noise Performance

Phase noise in oscillators is an important system consideration. Although these monolithic oscillators have low Q varactors which will be improved by process refinements, data is included for these circuits as a reference point.

A dual source measurement method was used with a very clean reference oscillator as the second source. The mixed output was then fed to a frequency discriminator which then drives a wave analyzer. Fig. 13 is the single-sideband phase noise in a 1-Hz bandwidth.

V. Conclusion

A design technique has been developed that allows oscillator bandwidth to be predicted and tradeoffs to be performed between circuit configurations and varactor ratio.

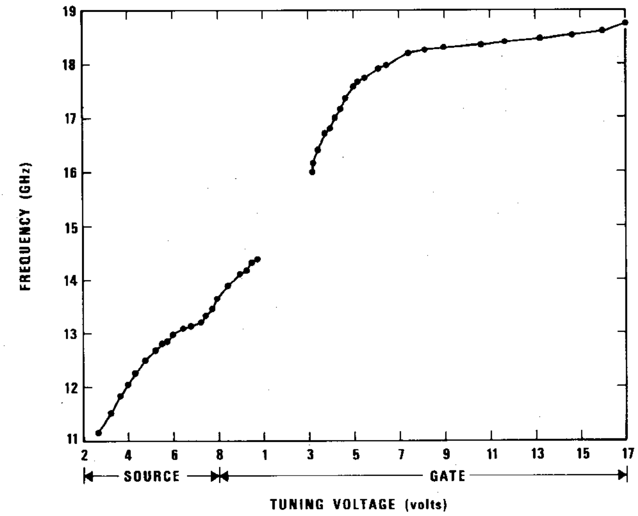

Fig. 11. Monolithic VCO tuning curve.

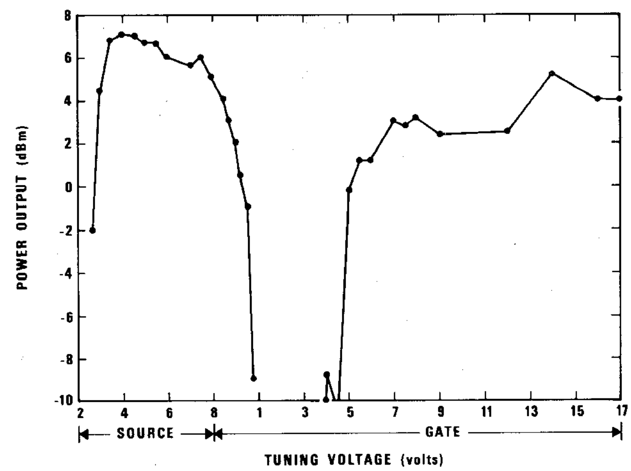

Fig. 12. Monolithic VCO power curve.

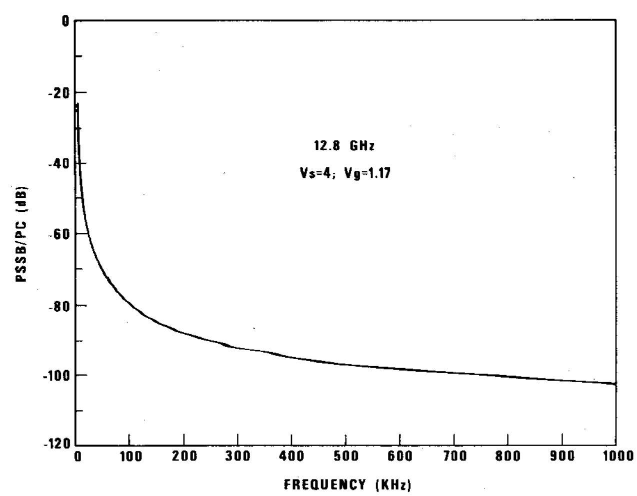

Fig. 13. SSB phase noise of monolithic VCO (1-Hz bandwidth).

Monolithic voltage tuned oscillators have been built on a 1.1-mm × 1.2-mm chip which included the 300-μm FET, two varactors, and all of the associated circuit elements except the 15- to 50-Ω output matching transformer. These circuits exhibited a tuning performance of 11.15 to 14.39

GHz and 16.0 to 18.74 GHz. This performance demonstrates the feasibility of covering octave bandwidths continuously using monolithic technologies. Assembly problems, size, and repeatability of present hybrid VCO's should be vastly improved once this technology matures.

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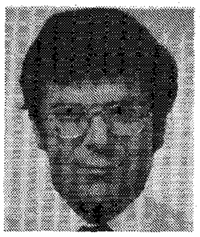

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In 1970 he joined TRW Semiconductor, R & D Department, Lawndale, CA, where he worked on GaAs IMPATT's and Si Schottky rectifier diodes. From 1972 to 1978 he was involved in the development of GaAs MESFET's and microwave diodes at Fairchild Semiconductor, Palo Alto, CA (1972–1974), Aertech Industries, Subsidiary of TRW, Sunnyvale, CA (1974–1977), and Rockwell International, Richardson, TX (1977–1978). Since 1978 he has been a Member of the Technical Staff of the Central Research Laboratories of Texas Instruments Incorporated, Dallas, TX. He is currently developing discrete GaAs MESFET's and GaAs monolithic microwave integrated circuits.

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An RF-Primed All-Halogen Gas Plasma Microwave High-Power Receiver Protector

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***Abstract*—A new type of keepalive for gaseous hybrid waveguide receiver protectors is shown to provide reliable and reproducible power limiting. The design allows halogen gases to be used in place of conventional gasfills, resulting in extremely fast recovery periods independent of duty cycle over a wide range. Recovery periods less than 100 ns were measured at incident power levels of 200-W peak at *X*-band frequencies using duty cycles up to 0.5.**

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I. Discussion

OVER THE 40-year history of gas discharge TR cells, many techniques have been used to supply initiatory electrons necessary for microwave pulse breakdown. The dominant technique has been the dc-excited keepalive [1],